A Novel Bipolar Series Ripple Compensation Method for Single-Stage High-Power LED Driver

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***Abstract*—It has been well documented that series compensation (SC) configuration can significantly reduce the total output capacitance of LED driver without sacrificing the power factor (PF), thus enabling the use of long-life film capacitors. Most importantly, SC provides the advantages over the parallel compensation (PC) methods in that it reduces the voltage stresses of the auxiliary stage components and thus can provide a higher efficiency, which is especially desirable for high-power LED drivers. However, with conventional series compensation, the auxiliary stage requires an auxiliary winding from the main stage. This increases the cost as well as the complexity of the circuit design. In this paper, a novel Full-Bridge Ripple Compensation Converter (FB RCC) using floating capacitor is proposed. By innovatively controlling the power flow of this auxiliary circuit, the auxiliary winding can be eliminated, thus making the input side of the auxiliary circuit floating and rendering a more cost effective and more flexible solution for both isolated and non-isolated LED driver applications. The new ripple compensation method retains the outstanding ripple-cancellation ability and high efficiency of the original SC method, and has been demonstrated in a 100W, 150V-0.7A experimental prototype.**

I. INTRODUCTION

The mainstream solution for AC-powered high-power LED drivers (V_{in}=85~265Vac, Po>50W), two-stage LED driver configuration, generally suffers from the lower power conversion efficiency since all the power is converted twice through this cascaded configuration[1]. Compared to the two-stage solution (given that the power factor requirements and the output capacitances are the same), single-stage solutions can save the energy but suffer from a low frequency current ripple. In conventional single-stage solutions, bulky high-capacitance capacitors are necessary to mitigate the current ripple. Otherwise, a periodic double-line-frequency light flickering occurs, which is visually harmful to humans[2, 3]. To maintain a high power density, electrolytic capacitors are necessary, which significantly reduce the life span of the entire LED bulb[4]. Several electrolytic-capacitor-less solutions have been proposed for single-stage LED drivers to replace the electrolytic capacitors with film capacitors[5] or ceramic capacitors[6-12], but they all have drawbacks.

A sub-harmonic injection method is proposed in [6]. This method reduces the required output capacitance at the cost of the power factor, because the sinusoidal input current shape is distorted by the current injection. A parallel compensation method [7-9] can achieve both high Power Factor (PF) and tight current regulation by adding an auxiliary power stage in parallel with the power factor correction (PFC) stage's output port to compensate the output current ripple, as shown in Fig. 1(a). However, the resulting high voltage stress on the auxiliary stage leads to high component costs and a relatively low efficiency. In addition, an output filter inductor L_O is required in series with the LED string. In [10, 11], a unipolar series compensation method is proposed. The component voltage stress is reduced to the peak to peak voltage ripple, as shown in Fig. 1(b). However, the room for capacitance reduction is still limited since the ripple compensation circuit is unipolar. In [12], a bipolar series compensation method is proposed to double the capacitance reduction ability (assume using the same type of switches) as the switches stress in the proposed method is reduced by half as compared to the unipolar one. However, the extra winding from the main stage as well as the diode (D_{aux}) not only increases the complexity of the circuit but also bring the extra loss.

Moreover, the existing SC methods are not ideal (it is suitable but with heavy design compromise) for the LED drivers with variable output voltage requirement. In order to adept different LED-load combinations, the drivers are expected to handle a wide output voltage range under the rated

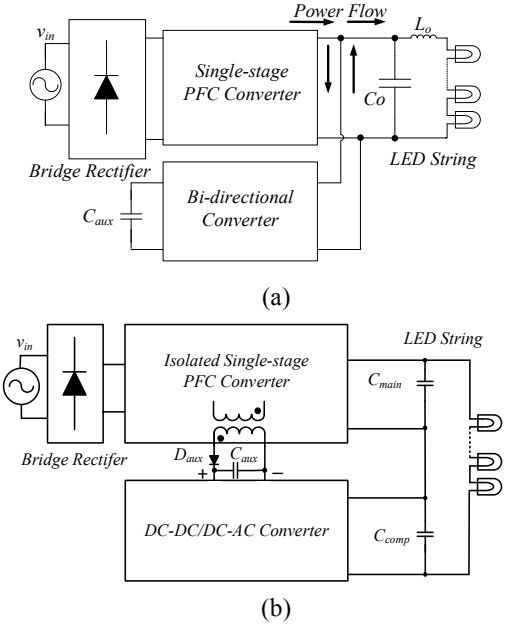


Fig. 1. Existing electrolytic-capacitor-less LED driver methods with an auxiliary stage. (a) Parallel compensation. (b) Existing series compensation.

output current. The ratio of the highest specification over the lowest specification is usually higher than 2 times (e.g. V_{LED}=60~150V). With the existing compensation technologies proposed in [10-12], given the auxiliary winding turn ratio is fixed, the component voltage rating has to be overdesigned under the low output voltage operation (e.g. V_{LED}<150V) to fit the voltage stress at the highest output voltage operation (e.g. V_{LED}=150V), resulting a non-optimal solution.

This paper proposes a single-stage LED driver configuration with Full-Bridge Ripple Compensation Converter (FB RCC) using a floating input capacitor. No auxiliary winding is required for this compensation stage, making it a more cost effective and more flexible solution applicable for both isolated and non-isolated LED driver applications. Furthermore, since the auxiliary transformer winding has been removed, the FB RCC input voltage is independent from the PFC stage output voltage and can be designed close to half of the PFC voltage ripple. In other words, the proposed FB RCC method avoids the overdesigning of the component voltage rating in the auxiliary stage at low output voltage operation for variable-output-voltage LED drivers.

This paper is organized as follows: Section II introduces the principle of the proposed method. Section III discusses the design of key parameter values. Section IV provides the experimental results and Section V concludes the paper.

II. PRINCIPLE OF THE PROPOSED METHOD

A. Proposed FB RCC Architecture Using a Floating Capacitor and Ripple Compensation

Fig. 2(a) shows two operational circuit stages in the bipolar series ripple compensation configuration: the single-stage PFC stage and the FB RCC. The PFC stage can be either isolated or non-isolated as the input-side capacitor in the auxiliary stage (C_{aux}) is floating.

When the input power factor is unity, the AC voltage ripple at double line frequency appears on the top of the DC voltage at the PFC stage output, shown as the upper red curve in Fig. 2(b). It is expressed in (1).

$$v_{main} = V_{DC} + v_{ripple} \tag{1}$$

Where v_{main} is the output voltage of PFC stage, and V_{DC} and v_{ripple} are the DC component and the double line frequency AC component of v_{main}, respectively. The output voltage of the FB RCC stage v_{comp} is an AC voltage shown as the middle blue curve in Fig. 2(b), which tracks v_{ripple}, as expressed in (2).

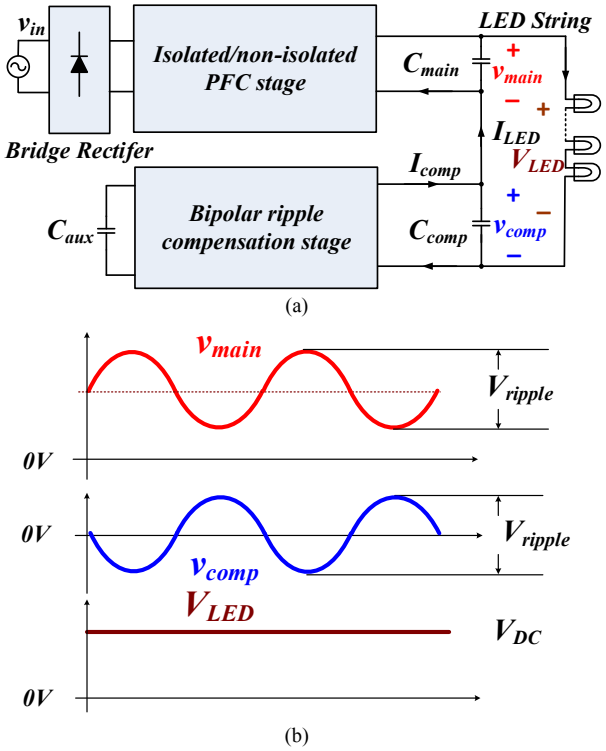


Fig. 2. Principle of proposed electrolytic-capacitor-less LED driver. (a) bipolar ripple compensated LED driver configuration. (b) Key waveforms.

$$v_{comp}(t) = -v_{ripple}(t) \tag{2}$$

As a result, the LED string sees only the DC component (V_{DC}) as shown in the lower brown line in Fig. 2(b).

$$V_{LED} = v_{main} + v_{comp} = V_{DC} \tag{3}$$

Since the high-power LED bulbs usually require electrical isolation, single-stage Flyback topology is selected for the PFC stage. Fig. 3 illustrates the proposed LED driver topology,

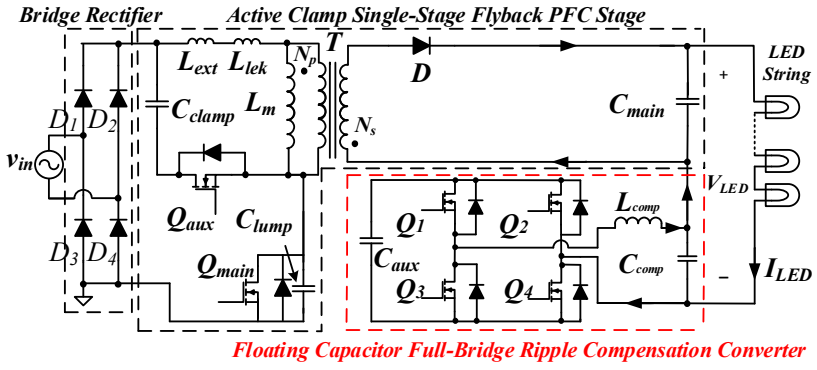


Fig. 3. Proposed electrolytic-capacitor-less LED driver architecture.

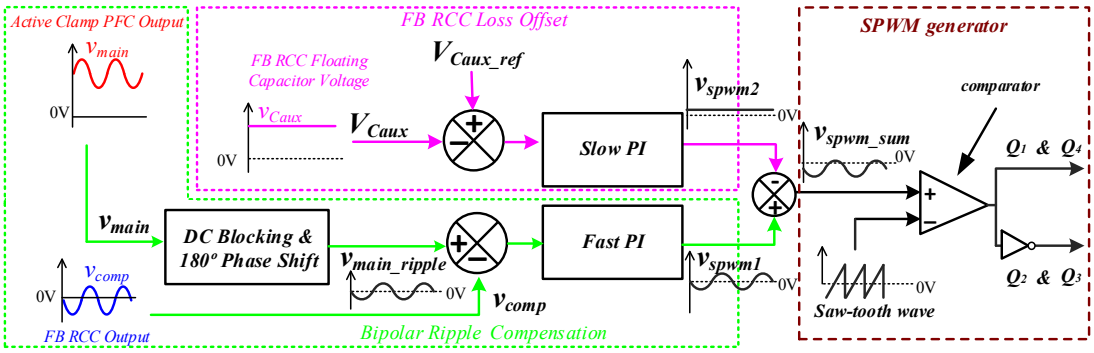


Fig. 4. Control strategy for the proposed floating Capacitor FB RCC stage.

where the FB RCC is highlighted. It is composed of four switches (Q_1~Q_4), one inductor (L_{comp}) and two capacitors (input capacitor C_{aux} and output capacitor C_{comp}). It is noticed that C_{aux} voltage contains 120Hz ripple while C_{comp} only filters out the high switching frequency noise as a part of output filter. The detailed C_{aux} design equations are given in Section III.B.

B. Basic Bipolar Ripple Compensation Loop

The complete control strategy for the proposed FB RCC stage is illustrated in Fig. 4, where the basic bipolar ripple compensation feedback loop is shown in the green box. The DC blocking and 180˚ phase shift circuit outputs the AC reference (v_{main_ripple}) for the FB RCC by blocking the DC component in v_{main}. Then a Sinusoidal Pulse Width Modulation (SPWM) control signal (v_{spwm1}) is generated based on this AC reference. With this loop, the FB RCC can build a reversed double-line-frequency AC voltage. Two operation modes of the FB RCC circuit are shown in Fig. 5.

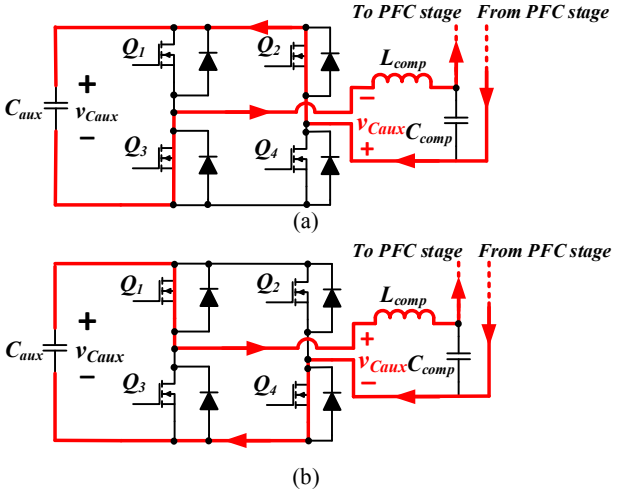


Fig. 5. Proposed bipolar FB RCC operation modes. (a) C_{aux} charging mode. (b) C_{aux} discharging mode.

The four MOSFETs Q_1~Q_4 conduct diagonally to provide paths for the LED current I_{LED}. When FB RCC output is higher than the reference, Q_2 and Q_3 are conducted while Q_1 and Q_4 are off; when RCC stage output is lower, Q_1 and Q_4 are conducted while Q_2 and Q_3 are off. This PI loop (shown as fast PI in Fig. 4) in the ripple compensation box features high bandwidth to provide a quick AC reference tracking ability.

C. FB RCC Loss Offset Loop and v_{Caux} Regulation

In a half-line cycle, when the output voltage of the main stage is greater than the LED reference voltage, the FB RCC stage will provide a negative voltage to cancel the ripple and the energy will flow into the FB RCC. When the output voltage of the main stage is smaller than the reference voltage, the FB RCC stage will provide a positive voltage to cancel the ripple and the energy will flow out of the FB RCC. If the FB RCC is lossless, the sum of the input energy and the output energy in a half line cycle will be equal, and thus the C_{aux} voltage will be self-balancing. However, the FB RCC has power loss in practice. If the C_{aux} voltage is not regulated, the input energy to the FB RCC stage will be less than the output energy in a half-line cycle, then the C_{aux} will be discharged and the C_{aux} voltage will drop. When the C_{aux} voltage is sufficiently low, the FB RCC stage can no longer produce the peak voltage required to cancel the main stage's ripple at valley points, and then under-compensation may occur. This phenomenon is shown in Fig. 6(a), where periodical bumps occur on top of LED DC voltage at double-line frequency.

To solve this problem, an extra control loop is added to regulate the average C_{aux} voltage, as shown in the purple box in Fig. 4. This loop allows the FB RCC to absorb slightly more input energy than the output energy in a half-line cycle in order to offset the energy loss. As a result, the C_{aux} voltage can be regulated and kept stable at its reference value (V_{Caux_ref}). The following inequality must be satisfied to achieve fully ripple compensation according to the electrical features of FB RCC topology.

$$v_{C_{aux}} \geq V_{comp\_pk} = \frac{1}{2} V_{ripple} \tag{4}$$

where v_{Caux} is the C_{aux} voltage which contains a 120Hz ripple component on the top of its average DC voltage. V_{comp_pk} is the peak value of the FB RCC output voltage (v_{comp}), which is decided by the peak to peak value of the main stage output voltage ripple (V_{ripple}).

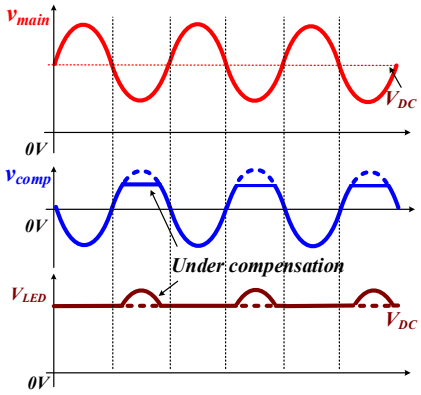
D. Control Strategy for the Floating Capacitor FB RCC

A combined control strategy is proposed for the FB RCC using a floating input capacitor. This control method is under the assumption that the loss in the FB RCC stage changes quite slow so that it can be considered as a DC value in one half-line cycle. This assumption is practical for a fixed-load LED driver.

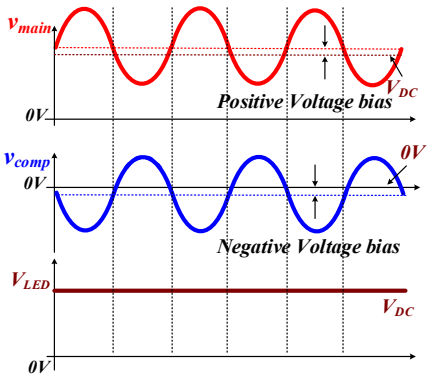
The two control loops in the proposed controller handle two tasks, separately: i. tracking the shape and magnitude of the periodic AC ripple and ii. compensating the FB RCC loss.

As shown in Fig. 4, the fast PI loop tracks the AC ripple reference (v_{main_ripple}) and provides an ideal SPWM control output (v_{spwm1}) while the slow PI loop regulates the floating capacitor voltage (V_{Caux}) which generates a DC control voltage (v_{spwm2}). These two control outputs are added together as v_{spwm_sum} and then compared to the saw-tooth wave to generate the SPWM driver signals for the four switches in the FB RCC stage, shown in brown box in Fig. 4. As a result, the FB RCC produces a reversed AC ripple voltage with a very small negative DC voltage bias, as shown in Fig. 6(b).

It should be noticed that this negative DC voltage bias in the FB RCC stage output (v_{comp}) will not affect AC ripple reference (v_{main_ripple}) and the normal operation of the fast ripple compensation loop because this is a DC signal (according to the assumption). All the DC information from the PFC output is blocked by the DC blocking circuit before it becomes the reference for the fast loop. Therefore, the reference signals of these two loops are decoupled and both of the two loops are able to operate stably and simultaneously.



(a)



(b)

Fig. 6. Under compensation analysis (a) without loss compensation loop. (b) with loss compensation loop.

E. PFC and LED Current Regulation

The LED current is regulated and the power factor correction (PFC) is achieved by using the control diagram in Fig. 7, where the LED current feedback loop is highlighted. The change of compensation signal v_{comp_p} at primary side can lead to the change of RMS input current, thereafter results in input power change and the DC output voltage (V_{LED}) change. The LED current (I_{LED}) is controlled by changing the DC component in the LED string voltage (V_{LED}). With a PFC controller, the LED current (I_{LED}) is regulated exactly equal to its reference by controlling the output voltage (V_{LED}).

Active clamp technology is applied to the PFC stage to achieve high system efficiency [13-15]. In fact, the FB RCC does not affect the DC value of V_{LED} and I_{LED} and only compensates the double-line-frequency AC component in the LED voltage. In this way, the LED voltage can be a pure DC voltage by using the FB RCC. At the same time, unity input power factor can be achieved by Flyback converter at the primary side.

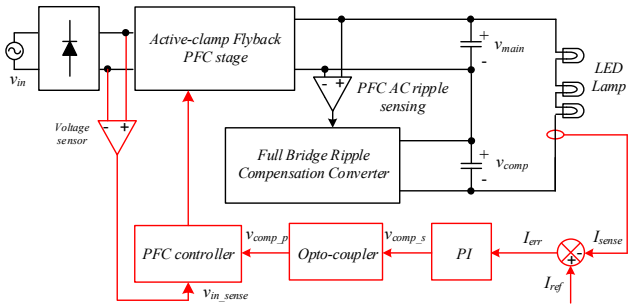


Fig. 7. PFC and output current controller

III. DESIGN OF KEY PARAMETER VALUES

A. Main Stage Output Capacitor C_{main}

The main stage's output capacitance value needs to be reduced in order to remove the electrolytic capacitors. However, minimizing the main stage's output capacitance and limiting the double line frequency voltage ripple is a trade-off, which affects the maximum voltage stress on the main stage's output capacitors and the voltage stress on the FB RCC stage's switches. The peak to peak value of the main stage's output ripple voltage V_{ripple} can be evaluated via the LED current, I_{LED}, and the output capacitance, C_{main}, as shown in (5).

$$V_{ripple} = \frac{P_{in}}{\omega \times C_{main} \times V_{LED}} = \frac{I_{LED}}{2\pi \times f \times C_{main}} \tag{5}$$

It is also observed from (5) that double-line-frequency voltage ripple amplitude, V_{ripple}, is determined by the LED current, I_{LED}, rather than the output voltage, V_{LED}, given the line frequency and PFC output capacitor are fixed. Therefore, the series ripple compensation can be achieved and under-compensation phenomenon can be avoided as long as the FB RCC stage input voltage, v_{Caux}, is regulated higher than the voltage ripple at the rated LED current, regardless of the PFC output voltage.

B. FB RCC Stage Floating Capacitor C_{aux}

To avoid the under-compensation phenomenon as shown in Fig. 6(a), the C_{aux} value is critical. The design should ensure that the voltage across C_{aux} is always higher than the auxiliary output voltage, v_{comp}, at any time instant.

Under the assumption that FB RCC is working at high frequency (f_{sw}>>f_{line}), the C_{aux} capacitance value is designed by the LED current (I_{LED}), the AC line voltage frequency (f_{line}), the allowed input voltage ripple (V_{Caux_ripple}), the average input voltage (V_{Caux_avg}) as well as the peak to peak output voltage of FB RCC (V_{ripple}). The expression is shown in (6).

$$C_{aux} \geq \frac{I_{LED} \cdot V_{ripple}}{4\pi \cdot f_{line} \cdot V_{C_{aux\_avg}} \cdot V_{C_{aux\_ripple}}} \qquad (6)$$

The capacitor C_{aux} selected based on (6) will ensures that the FB RCC output completely cancel the ripple component in LED string current, I_{LED}. The detailed derivation is shown in APPENDIX at the end of the paper.

IV. EXPERIMENTAL VERIFICATION

The key parameters of the experimental LED driver are given in Table 1.

Table 1. Prototype Parameters Values

Specifications of LED driver	
Line input voltage (v_{in})	85~265V
LED output voltage (V_{LED})	≈150V
LED output current (I_{LED})	0.7A
Out power (P_O)	100W
Line frequency (f)	60Hz
Active Clamp Single-stage Flyback PFC Stage	
Output Capacitor (C_{main})	56 μF (250V Film Cap)
Switches (Q_{main} Q_{aux})	SPP11N80C3
Diode (D)	C3D16060
Turns Ratio (N_p:N_s)	1.2:1
Magnetizing Inductance (L_m)	1300 μH
Internal Leakage Inductor (L_{lek})	33 μH
External Leakage Inductor (L_{ext})	15 μH
Active Clamp Capacitor (C_{clamp})	68 nF×4 (400V Film Caps)
Single-stage PFC Controller	NCP1652A
Proposed FB RCC stage	
Switching Frequency (f_{sw})	156 KHz
Floating Input Capacitor (C_{aux})	10 μF×10 (50V 1206 Ceramic Cap)
Output Inductor (L_{comp})	50 μH
Output Capacitor (C_{comp})	4.7 μF (50V 1206 Ceramic Cap)
MOSFETs (Q_1~Q_4)	TPN11003NLLQ×4 (30V, 11mΩ)
LED String Load	
LED Chip Part Number	XMLEZW-02-0000-0B00T527F×27
Forward Voltage/pcs (V_f) Typ	6 V
Max Current (I_{max})	2 A
Luminous Flux/pcs @ 670 mA	270 lm

The PFC stage output capacitor (C_{main}) is selected as 56 μF, so that peak to peak value of PFC output voltage ripple (V_{ripple}) is 34V, according to (5), which is equal to the peak to peak output voltage of FB RCC.

In order to satisfy the inequality (4), the average value of the floating capacitor voltage, V_{Caux_avg}, is selected as 35V with a maximum 10V peak to peak ripple, V_{Caux_ripple}. So that the allowed minimum input voltage is 30V which is a reasonable value to ensure the bipolar compensation of the FB RCC.

All the parameters for C_{aux} design are listed in Table 2.

Table 2. C_{aux} design Parameters

T_{sw}	V_{ripple}	V_{Caux_avg}	V_{Caux_ripple}
1/156kHz	34V	35V	10V

Substituting the values in Table 2 into equations (6) yields a minimal requirement (C_{aux}≥91μF) for FB RCC input capacitance (C_{aux}) to avoid under compensation phenomenon.

C_{aux} is selected as 100μF in the prototype (10μF×10 pieces 50V 1206 Ceramic Caps).

Fig. 8 shows that the FB RCC stage input voltage v_{Caux} is regulated at 35±5V by the proposed loss offset loop. The FB RCC stage exhibits a slight negative DC voltage bias of 1.2V at the FB RCC stage output voltage. This experimental result validates the previous analysis for Fig. 6(b).

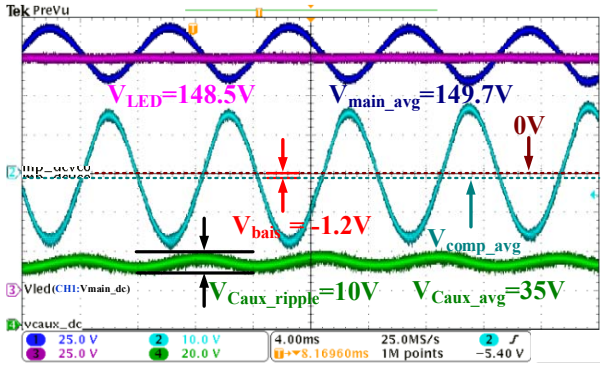
Fig. 9 shows the input voltage and input current waveform of proposed compensation method (v_{in}=110Vac), which has achieved a high PF of 0.994. Fig. 10 (a) shows that the proposed compensation method produces a smaller LED driving current ripple @120Hz (7.8mA RMS) with only 60.7μF total output capacitance(C_{main}+C_{comp}), compared to a higher 8.2mA RMS current ripple in the conventional single-stage LED driver, where 4700μF output capacitance is required, shown in Fig. 10(b). Therefore, the total required output capacitance of conventional signal-stage solution is reduced by 98.7%! Also, it should be noticed that only C_{main} is of high voltage rating while both C_{comp} and C_{aux} are low-voltage-rating components.

Meanwhile, the experimental prototype yields the system efficiency of 91%, when v_{in}=110Vac. More experimental results under the universal AC input are shown in Fig. 11, where a peak system efficiency of 92.5% has been achieved. The FB RCC stage loss is generally less than 1% under different input voltage, as shown in Fig. 12.

Dimming performance of the proposed LED driver is also measured and shown in Fig. 13. According to the experimental results, the half-load (P_O=50W, V_{LED}≈150V) system efficiency are generally higher than 88.5% and the PF are over 0.9 under both the nominal input voltages (110Vac and 220Vac).

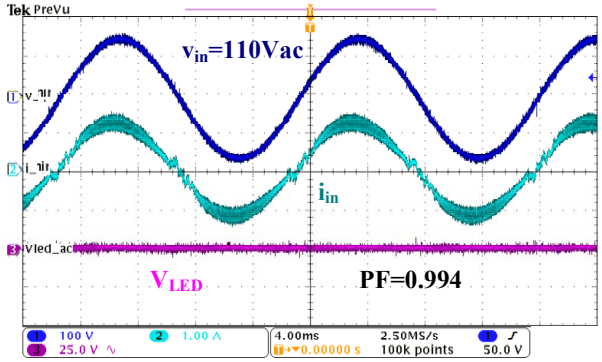
V. CONCLUSIONS

This paper proposes an electrolytic-capacitor-less with bipolar series ripple compensation (FB RCC) solution using a floating input capacitor for single-stage high-power LED driver. It features very low voltage stress, very small output capacitance, and very low LED driving current ripple. It is applicable to both isolated and non-isolated single-stage LED drivers. The required total output capacitance is only 1.3% of conventional methods, and thus electrolytic capacitors can be removed.



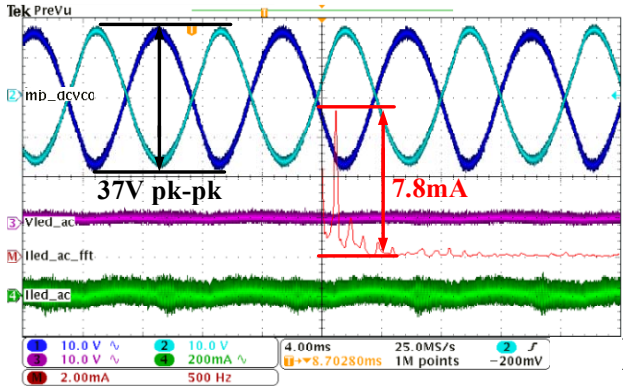
CH1: PFC stage output voltage (v_{main})CH2: FB RCC output voltage (v_{comp})
CH3: LED string voltage (V_{LED}) CH4: FB RCC floating cap voltage (v_{Caux})

Fig. 8. Key experimental waveforms of proposed FB RCC, when V_{in}=110Vac, V_{LED}≈150V, I_{LED}=0.7A, P_O=100W

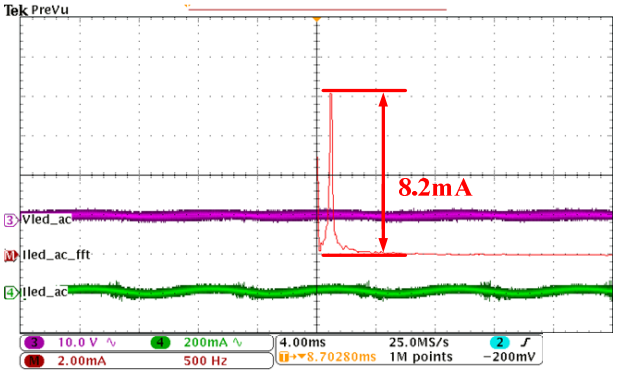


CH1: AC input voltage (v_{in}) CH2: AC input current (i_{in})
CH3: LED string voltage (V_{LED})

Fig. 9. Input current and output voltage of the proposed LED driver, when V_{in}=110Vac, V_{LED}≈150V, I_{LED}=0.7A, P_O=100W



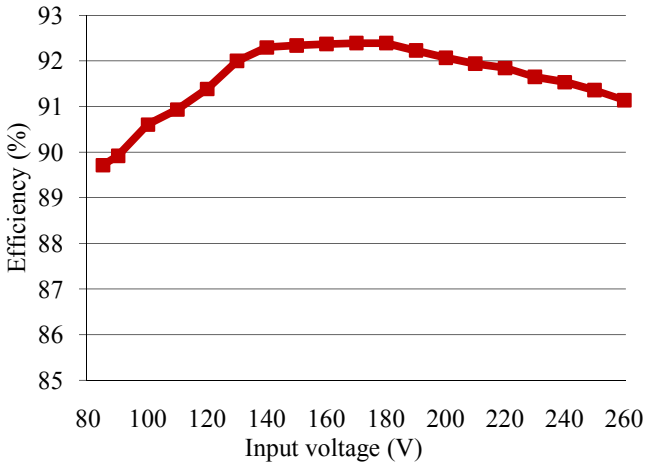
(a) single-stage PFC+ FB RCC configuration: (C_{main}=56μF,C_{aux}=100μF,C_{comp}=4.7μF)



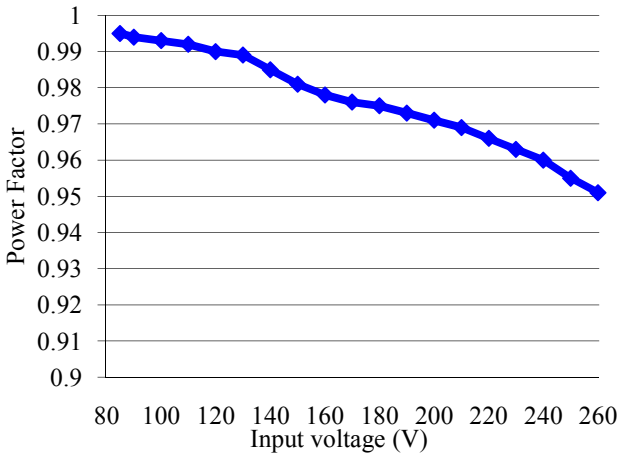
(b) Conventional single-stage configuration: C_O=4700μF

CH1: AC coupled PFC stage output voltage (v_{main}:10V/div) CH2: FB RCC output voltage (v_{comp}:10V/div) CH3: AC coupled LED lamp voltage (V_{LED}:10V/div)
CH4: AC coupled LED lamp current (I_{LED}:200mA/div) CHM: FFT of AC coupled LED current (I_{LED_FFT}:2mA/div)

Fig. 10. Compensation performance of the proposed LED driver, when V_{in}=110Vac, V_{LED}≈150V, I_{LED}=0.7A, P_O=100W.



(a) System efficiency.



(b) Power factor.

Fig. 11. Performance of the proposed LED driver with FB RCC at full load, when C_{main}=56 μF, V_{LED}≈150V, I_{LED}=0.7A, P_o=100W.

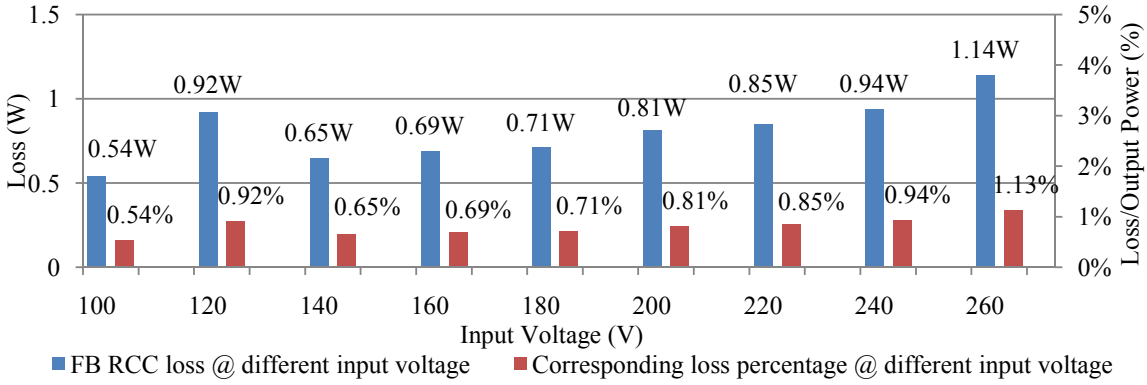
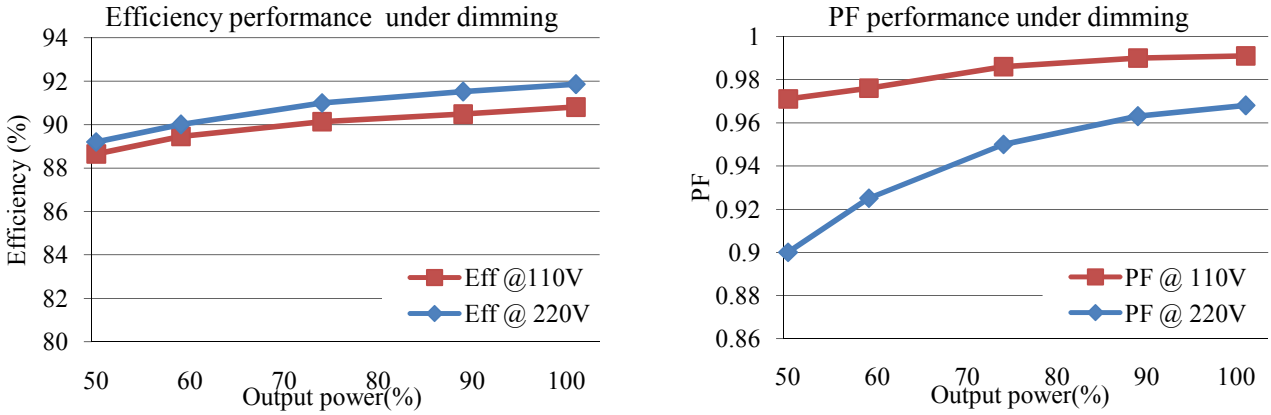


Fig. 12. FB RCC stage loss in proposed LED driver when V_{LED}≈150V, I_{LED}=0.7A, P_o=100W.



(a) System efficiency.

(b) Power factor.

Fig. 13. Dimming Performance of proposed LED driver with FB RCC, when C_{main}=56μF, V_{LED}≈150V.

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APPENDIX

A. FB RCC floating capacitor C_{aux} design rule derivation:

The instant C_{aux} input voltage is composed of a DC average voltage and a varying double-line-frequency voltage ripple resulting from the charging and discharging of the capacitor by the load current, I_{LED}.

$$v_{C_{aux}} = V_{C_{aux\_avg}} + v_{C_{aux\_ripple}} \tag{7}$$

According to the operation modes of compensation stage, the floating input capacitor is charged when Q_2 and Q_3 are conducted (Q_1 and Q_4 are off) and it is discharged when Q_1 and Q_4 are conducted (Q_2 and Q_3 are off). These two intervals are shown in the following equations, separately.

$$T_{charge} = T_{sw} \cdot (1 - D) \tag{8}$$

$$T_{discharge} = T_{sw} \cdot D \tag{9}$$

where T_{sw} is the switching period of compensation stage. D is duty cycle of the driving signals for Q_1 and Q_4, shown in the following equation.

$$D(t) = \frac{1}{2} + \frac{1}{2} \cdot M \cdot \sin(2\omega t) \tag{10}$$

where ω is angular frequency of line voltage and M is the modulation index of SPWM, expressed as (11).

$$M = \frac{\frac{1}{2} V_{ripple}}{V_{C_{aux\_avg}}} \tag{11}$$

Since the average current going through the switches is fixed by the load, the difference between charging time and discharging time of each switching cycle determines the behavior of input current, leading to the increase or decrease of the input voltage. The charge for each cycle can be expressed by the following equation.

$$\begin{aligned} &Q_{discharge}(t) \\ &= I_{LED} \cdot (T_{discharge}(t) - T_{charge}(t)) \\ &= I_{LED} \cdot M \cdot T_{sw} \cdot \sin(2\omega t) \end{aligned} \tag{12}$$

The sum of discharge is expressed in the following equation.

$$\begin{aligned} &Q_{discharge\_sum}(nT_{sw}) = \sum_{t=0}^{nT_{sw}} Q_{discharge}(t) \\ &= \sum_{k=1}^{n} I_{LED} \cdot M \cdot T_{sw} \cdot \sin(2\omega \cdot kT_{sw}) \end{aligned} \tag{13}$$

According to the characteristics of the two-level SPWM modulation strategy, the discharging period is always longer than the charging time during the first half line cycle before it enters the other half line cycle. Therefore, the floating input capacitor keeps discharging over each switching cycle and the voltage keeps decreasing until it touches the valley at the half cycle point. Then, the biggest voltage drop can be calculated in the following equation.

$$V_{C_{aux\_ripple}} = \frac{Q_{discharge\_sum}(\frac{T_{line}}{4})}{C_{aux}} \tag{14}$$

In fact, this is the worst case because the output voltage is on the peak value simultaneously.

$Q_{discharge\_sum}(T_{line}/4)$ in (14) can be simplified into (15) after the mathematical deduction.

$$\begin{aligned} &Q_{discharge\_sum}(\frac{T_{line}}{4}) \\ &= \sum_{k=1}^{\frac{T_{line}}{4T_{sw}}} I_{LED} \cdot M \cdot T_{sw} \cdot \sin(\frac{4\pi T_{sw}}{T_{line}} k) \\ &= \frac{I_{LED} \cdot M \cdot T_{sw}}{\tan(\frac{2\pi T_{sw}}{T_{line}})} \end{aligned} \tag{15}$$

Since $T_{sw} << T_{line}$ ($f_{sw} >> f_{line}$),

$$\tan(\frac{2\pi T_{sw}}{T_{line}}) \approx \frac{2\pi T_{sw}}{T_{line}} \tag{16}$$

Then (15) can be further simplified, as shown in (17).

$$Q_{discharge\_sum}(\frac{T_{line}}{4}) = \frac{I_{LED} \cdot M}{2\pi \cdot f_{line}} \tag{17}$$

where f_{line} is the AC line voltage frequency.

Therefore, FB RCC is able to work normally for the whole line cycle as long as the input valley voltage is set higher than the peak output voltage. The final floating input capacitor C_{aux} design rule is shown in (18).

$$\begin{aligned} C_{aux\_min} &\geq \frac{Q_{discharge\_sum}(\frac{1}{4} T_{line})}{V_{C_{aux\_ripple}}} \\ &= \frac{I_{LED} \cdot V_{ripple}}{4\pi \cdot f_{line} \cdot V_{C_{aux\_avg}} \cdot V_{C_{aux\_ripple}}} \end{aligned} \tag{18}$$